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# Design of a Current Sensor for $I_{DDQ}$ Testing of CMOS IC

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**Abstract:** This study presents the design of an off-chip current sensor for $I_{DDQ}$ testing of CMOS (Complementary Metal-oxide Semiconductor) ICs (integrated circuit). It provides a linear voltage signal of $I_{DDQ}$ current with a conversion factor of 5 mV/μA without any amplification. A voltage-controlled switch is used to bypass the transient current peaks. It has also been shown that the sensor is capable of detecting $I_{DDQ}$ faults of a circuit at 100 kHz test frequency without degrading its performance.

**Key words:** $I_{DDQ}$ Testing, CMOS IC, Current Sensor

## INTRODUCTION

With the advent of semiconductor technology, a new era has begun in microelectronics. Electronic equipments and products have become part and parcel of our daily life [1]. Zero failure, high reliability and longevity are major business issues as well as customer expectation for the electronic goods. In many applications, accuracy and high reliability is essential and even life critical, for example, medical, aerospace etc. The key components of an electronic product are integrated circuits (ICs). In IC manufacturing, various physical defects may occur during the numerous physical, chemical and thermal processes [2].

Dramatic improvement of integration technology in IC manufacturing is rapidly leading to exceedingly complex, multi-million transistor chips. All the functionalities of an electronic system are being integrated on a single chip in less than 2 cm square silicon area. This growth is expected to continue full force for the future years. With the increase of such integration densities and complexities, problems associated with testing of ICs such as test generation, testing time, testing speed, testing cost, test scheduling, test access mechanism, controllability of the inputs, observability of the outputs etc. have become much more complex and acute. The cost of testing has become a major portion of the total cost of an electronic product. It is predicted in a survey that it will soon cost more to test a transistor than to make it [3].

Last few decades, functional testing was normal practice in the IC manufacturing industry for testing IC. But it has been seen that there are some physical defects usually in CMOS ICs such as gate oxide shorts, node bridges, etc. that cannot be detected by functional testing. With the presence of these defects, an IC may fail anytime while in operation. $I_{DDQ}$ testing has been proposed to overcome this problem [4]. Logic testing is still required to verify the functionality of the ICs and $I_{DDQ}$ testing improves the reliability of the testing. $I_{DDQ}$ testing measures the quiescent power supply current of an IC using suitable current sensor and the fault presence causes higher magnitude of $I_{DDQ}$ than the specified threshold value. There are two basic types of current sensor, on-chip current sensor and off-chip current sensor. The off-chip sensor offers more versatility and they can be combined with automatic test equipment (ATE).

**Design Requirements for the Sensor:** Specifications for a current sensor to be used in $I_{DDQ}$ testing are briefly discussed below:

**Current Measuring Frequency:** Regarding measuring frequency, the higher rate provides higher throughput. However, for higher frequency the accuracy in measurement should be concerned. For off-chip sensor, 10-100 kHz testing frequency is more realistic.

**Current Handling Property:** CMOS circuits draw current during the input digital logic changes. Typical transient current peaks for VLSI circuits can have of around 1 A [5]. After transient period, the power supply current is negligible (a few or less μA) and this current is known as $I_{DDQ}$. $I_{DDQ}$ current for a typical defective VLSI circuit is up to 1 mA [6]. So the sensor should be able to sense the quiescent current with precision. This is described as "listening for a pin drop immediately after a common shot" [7].

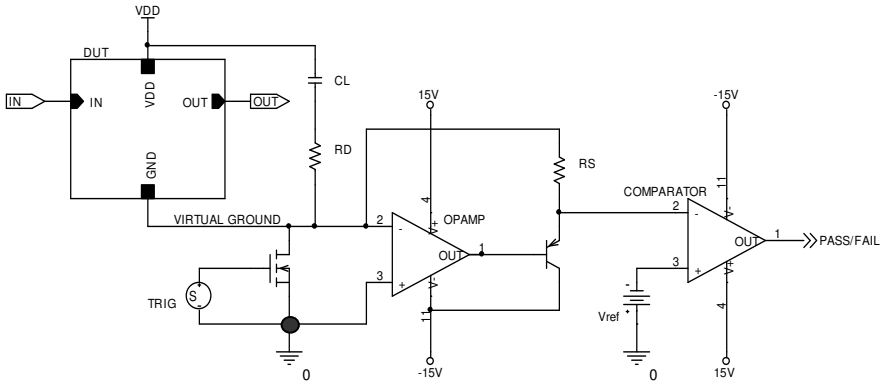


Fig.1: Schematic Diagram of the Current

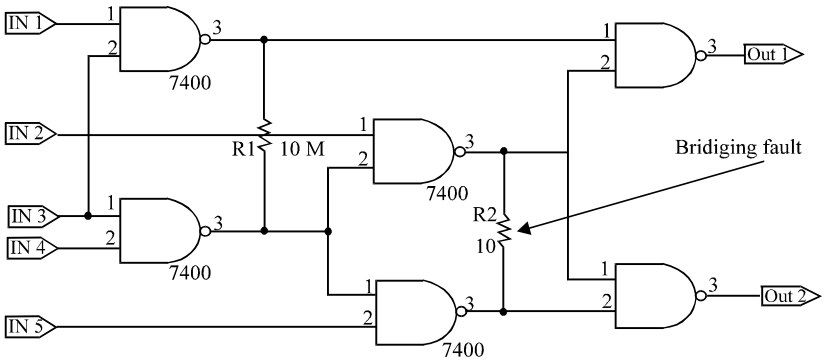


Fig. 2: c17 Benchmark Circuit with Bridging Faults Between Two Logic Elements

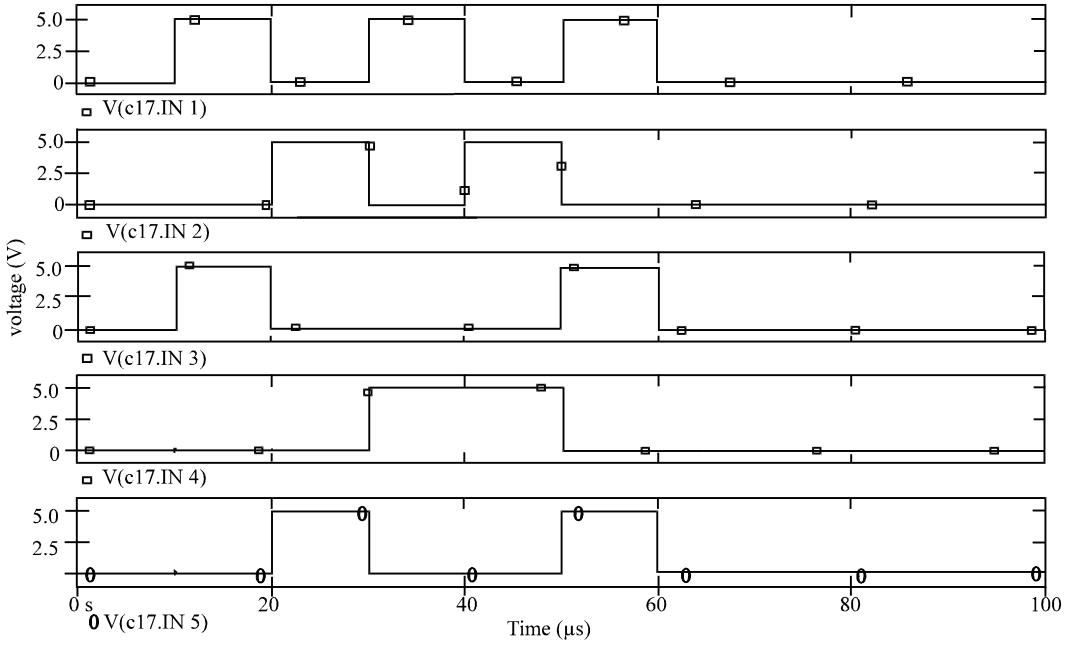


Fig. 3: 60 µs Input Waveform for the Benchmark Circuit "c17"

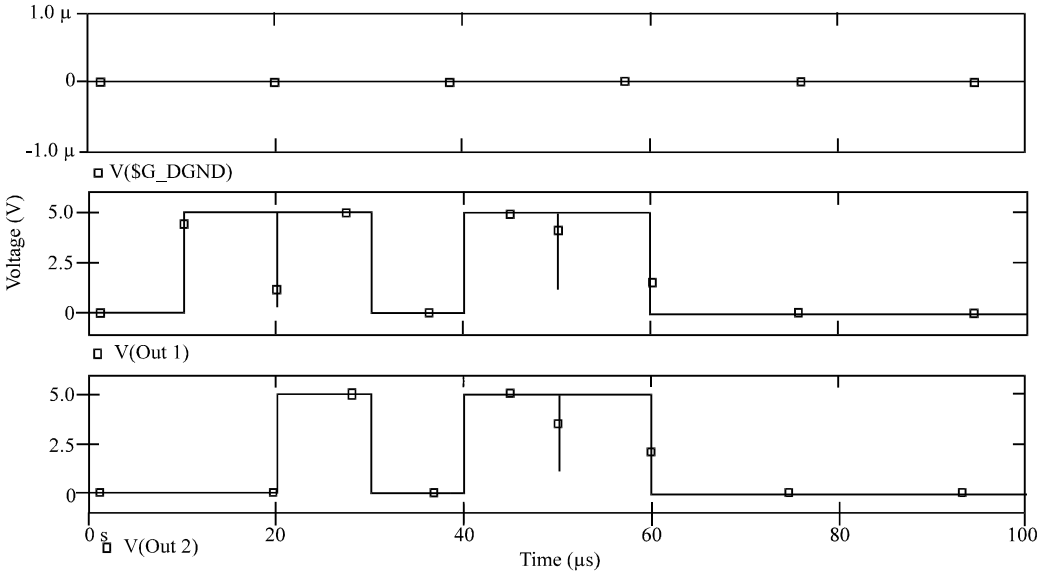


Fig. 4: Response of Fault-free DUT Without Current Sensor

**Effect on DUT:** The sensor should have minimum effect on device under test (DUT). This means that the sensor should be capable of maintaining proper power supply voltages across the DUT during testing. Specially during transient states, the $V_{DD}$ or GND level may shift due to large current. This can result in great performance degradation of the DUT and sometimes even cause ground bounce problems that may malfunction the DUT. Therefore the sensor should ensure negligible effect on DUT so that the DUT can operate properly.

**Design of the Sensor:** The design of the current sensor circuit with DUT is shown in Fig. 1. It has been designed using Capture CIS of the OrCAD (release 9.1) EDA software. The Enhancement-mode Power MOSFET has been chosen as the voltage-controlled switch (VCS) to bypass the high transient current peaks during switching the logic inputs. The max allowable high transient current peaks is ≈98A due to the Power MOSFET characteristics $I_D$ versus $V_{DS}$ when $V_{GS}$=5V. To ensure the transistor is ON during transient states, the triggering input with 60 µs pulse width is applied to the gate-to-source voltage of the transistor.

The operational amplifier (OP-AMP) is used to maintain the virtual ground at the DUT's ground pin so that ground level does not shift during $I_{DDQ}$ measurement. After switching off the bypass transistor, the quiescent current is guided to flow through the sense resistor Rs causing a proportional voltage drop across it. Since it is used as a feedback loop to OP-AMP, a linear current-to-voltage signal conversion is provided by the OP-AMP to the comparator. Some dead short circuits between $V_{DD}$ and ground can cause excessive $I_{DDQ}$ demanding very large voltage drop across $R_S$. But the maximum allowable voltage drop across $R_S$ is limited by negative power supply voltage of the comparator.

The PNP common-collector/emitter follower configuration is used, such that the output voltage of the current measurement circuit is equal to the voltage drop across $R_S$. In this design, $R_S$ is a load resistance of the common-collector configuration. Thus the output voltage of current measurement circuit is proportionally to the $I_{DDQ}$. It also used to bypass the quiescent current.

The comparator compares this voltage with the reference voltage ($V_{ref}$) to indicate whether the $I_{DDQ}$ is greater than the allowable magnitude or not. The maximum allowable $I_{DDQ}$ for a fault-free CMOS IC is 100 µA [2]. Thus the $I_{DDQ}$ current higher than 100 µA is considered as fault. It should be noted that in real hardware the sensor should be within a few millimeter of the DUT. This is to minimize the parasitic inductance and to optimize the decoupling system [6]. Otherwise the measurement frequency and the accuracy of the sensor may be affected.

**Verification Results:** ISCAS85 benchmark circuit "c17" has been used to verify the functionality and performance of the current sensor. The "c17" benchmark circuit consists of 6 NAND gates, 5 input pins and 2 output pins. For CMOS circuit, MOSIS 2µm technologies have been used with aspect ratio (W/L) of each PMOS is 3.6/2 µm and NMOS is 1.2/2 µm. The circuit diagram is shown in Fig. 2 with two bridging faults between two logic elements without feedback. Practically, small percentage of bridging faults having resistance value above 500 Ω in ICs and the higher the bridging resistance faults the more difficult to detect. The resistance values have been chosen very low (10 Ω) and very high (10M Ω) to show the ability of the current sensor to detect bridging faults of wide range.

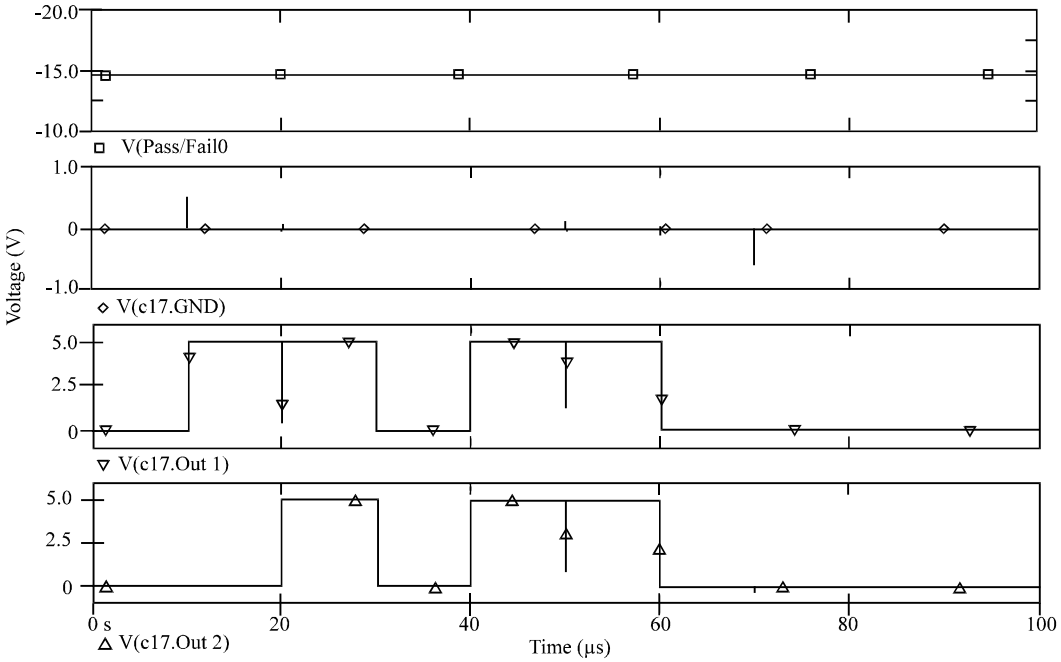


Fig. 5: Response of Fault-free DUT with Current Sensor

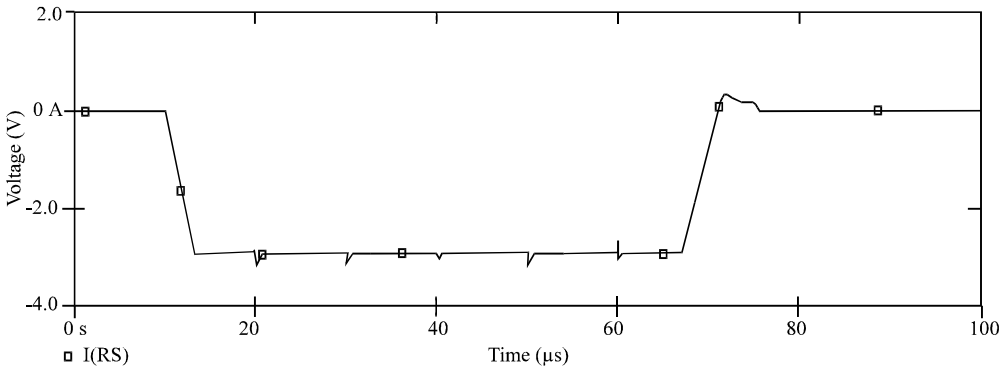


Fig. 6: Simulation Results Showing Fault-free $I_{DDQ}$ without VCS

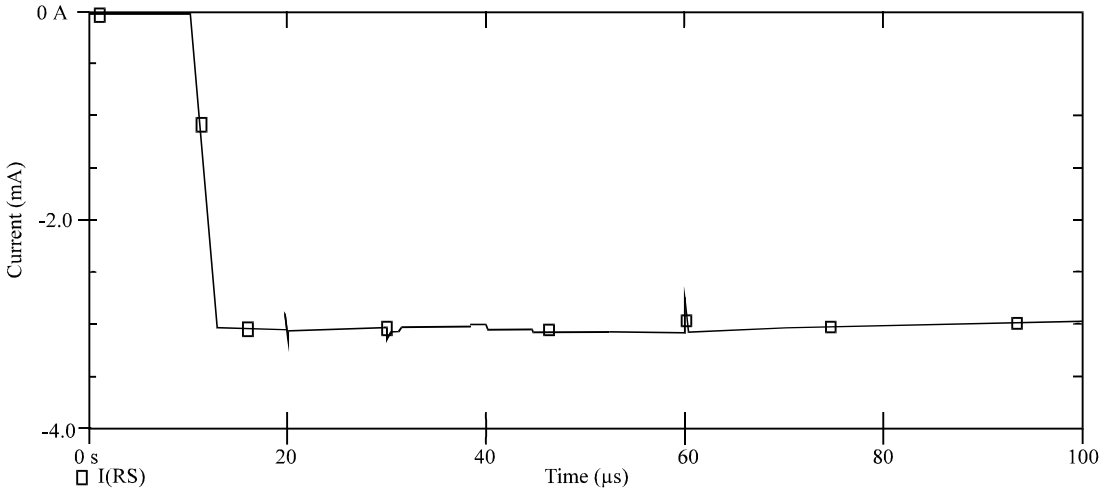


Fig. 7: Simulation Results Showing Faulty $I_{DDQ}$ Without VCS

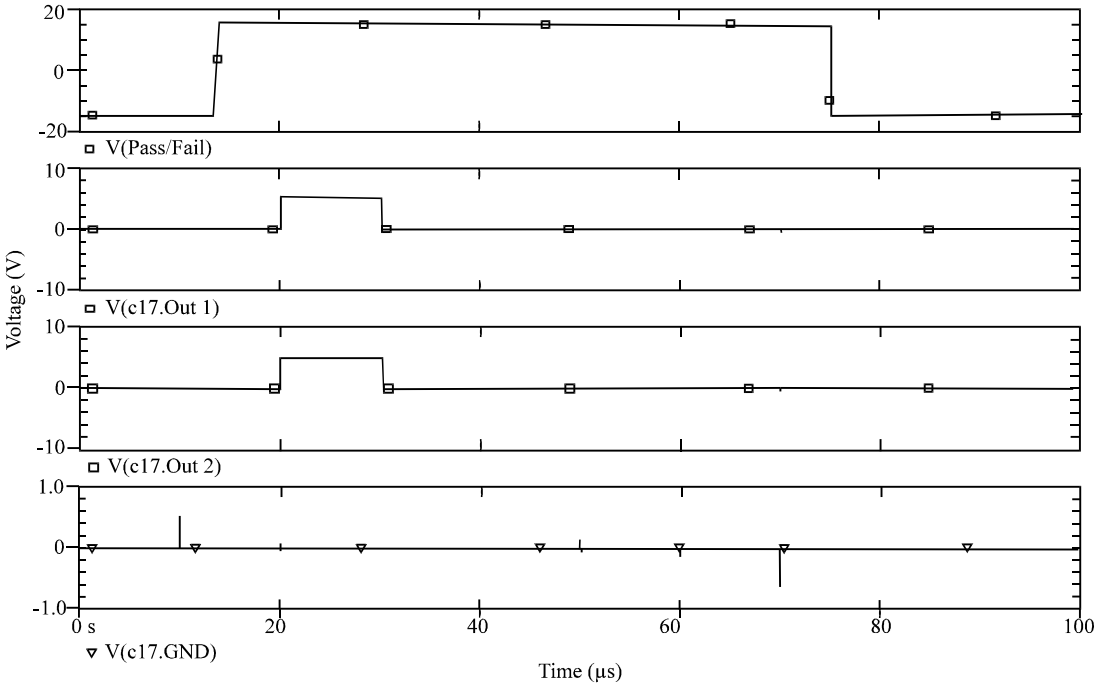


Fig. 8: Simulation Results of the Current Sensor with DUT Having Bridging Fault

The random input waveforms of 60µs duration have been shown in Fig. 3. The output voltages and ground level for fault-free DUT without connected to the current sensor is shown in Fig. 4. The waveform pattern changes after every 10 µs indicates the testing frequency is 100 kHz.

Response of the fault-free DUT with current sensor is presented in Fig. 5. The similar output wave shape as shown in the Fig. 4 and that in the Fig. 5 indicates that the presence of current sensor does not degrade the normal operation of the DUT. At the time of the bypass transistor switching, some spikes may appear at the ground pin of the DUT. To keep the magnitudes of these spikes in a reasonable limit and to filter the high impedance noise at high frequencies, the capacitor $C_L$=0.25 µF is used. However the value of $C_L$ is critical. It should be chosen in a very minimum range (<10 µF) to avoid distorted current measurement and degrade the measurement speed. Since DUT is fault-free, output voltage for the current sensor is low.

Figure 6 and 7 shows the simulation results of the sensor in transient condition. It indicates performance of the current sensor and determine its specifications. In Fig. 6 the transient current peak for this circuit is ≈3 mA in duration time of 10 to 90 µs when input digital logic changes. In Fig.7, it is clearly shown that the quiescent current does not return to its initial low value after the transient states (when input logics changes) indicate the DUT has faults.

In $I_{DDQ}$ testing, it is very significant to determine or specify the magnitude of maximum fault-free $I_{DDQ}$ as the threshold value for current measurement. However as stated earlier, it is difficult to determine the exact value of the threshold value. Therefore for this simulation, the threshold value will be depends on the current flow through $R_S$ as the specified maximum fault-free $I_{DDQ.}$ Figure 8 indicates the magnitude of maximum fault-free $I_{DDQ}$ for this circuit is ≈100 µA. Therefore, if the DUT draws more than 100 µA in quiescent states, the sensor should affirm it as faulty.

We have used the value of $R_S$ as 5kΩ, so that the reference voltage ($V_{REF}$) at the + input terminal of the comparator is - $(5\times10^{3}\times100\times10^{-6})$=-0.5 V. Any more than 100 µA will cause more negative voltage than $V_{REF}$ and the comparator output V (PASS/FAIL) will become high to indicate the fault. To prevent and to keep oscillation of $I_{DDQ}$ current at a minimum level, a damping resistor, $R_D$ is connected in series with $C_L$. This resistance must be chosen at a minimum level to minimize the effect of RC loading at the output; hence the circuit takes short time to stabilize.

Detection of bridging faults using the current sensor has been presented in Fig. 8. It shows that the sensor is capable of detecting bridging faults of wide range. These defects will create an opposite logic across the fault when applying an input vectors at DUT's inputs terminal. By comparing the output waveform with fault-free circuit, the opposite logic appears across 10MΩ resistance in time duration 10-20 µs and 10 Ω resistance in time duration 40-50 µs. In time duration 50-60 µs opposite logic appears across both of them. The simulation results also shows high V (PASS/FAIL)

for the desired duration and the DUT ground level is still maintained at '0' level even at duration faults occur.

The simulation results as shown in the Fig. 3 to 8 are with respect to 'c17' ISCAS85 benchmark circuits. The current sensor is also capable of detecting the faults of other DUT. It can be verified by carrying out the similar procedure using the simulation technique.

## CONCLUSION

Design of an off-chip current sensor is presented. Simulation results prove that the normal operation of the DUT with the current sensor does not degrade during testing and the testing frequency is around 100kHz. The current sensor is capable of detecting fault- $I_{DDQ}$ faults in a circuit with precise accuracy.

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