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DESIGN OF HIGH-SPEED PARALLEL IN PARALLEL OUT SHIFT REGISTER USING ALGAAS/GAAS MODFET TECHNOLOGY

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ABSTRACT

This study enumerates the efficient design and analysis of Parallel In Parallel Out (PIPO) shift register using AlGaAs/GaAs MODFET D flip-flop. The transient and power analysis are obtained with operating voltage at 1.3 V for the D flip-flop and PIPO shift register using pspice tool. There are many issues facing while integrating many number of transistors like delay, power dissipation, scaling of the transistors. To overcome these problem by Considered the AlGaAs/GaAs MODFET have promising application in the field of electronics. The simulation results are done and the power consumptions and delay are compared with the conventional MOSFET design. The comparison of results the MODFET based design is capable of efficient power savings.

Keywords: Flip-Flop, Shift Register, High-Speed, PIPO, MODFET, Delay, PDP, Power Consumption

1. INTRODUCTION

The system on chip designs will integrate hundreds of million transistors are dumped into a one chip, whereas the packaging and cooling both have a limited ability to remove the excess heat, So large amount of heat should not be dissipated. This low power design is need today's integrated systems and the switching speed is very important. The propagation delay is less compare with other existing work (Sridevi and Jayanthy, 2012; Kandukuru and Prakasam, 2012). The low power design is employed for the applications operated by batteries such as digital calculators, mobile phones, wrist watches, laptops and palmtops. The development of microelectronics takes time which is even lesser than the average life span of a human and yet it has seen as more than five generations. Since the year 1960's the low density fabrication process classified under small scale integration in which transistor count was limited to about 10. This rapidly gives way to medium scale integration in the late 60's when around 100 Transistors could be placed on a single chip. It is important to improve the battery life as much as possible. As the feature size of Complementary Metal Oxide Semiconductor (CMOS) technology process featured down According to Moore's Law, the designers are able to integrate many numbers of transistors onto the same die. The increase in number of transistors will primarily increase the probability of reliability issues. The Heat is one of the phenomenon packaging challenges in this area; it is one of the main challenges of low power design Methodologies and practices. Another driver of low power research is the reliability of the integrated circuit. Due to more switching implies higher average current is expelled and therefore the probability of reliability issues occurring rises. The most vital prime mover of low power research and design is our convergence to a Mobile society. We are moving from laptops to tablets and even smaller digital products. In this the profound trend continuing and without a match trending in battery life, the more low power issues will have to be addressed. This exhibits that low power tools and methodologies have to be developed and should be used in many number of applications. Wang and

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Robinson (2010) describes that the current trends will primarily mandate low power design automation on a very large scale to satisfy the trends of power consumption of today's and future integrated chips. Sharma *et al*. (2009) describes that the power consumption of very large scale integrated design is given by generalized relation, $P = CV^2f$. Since power value is proportional to the square value of the voltage as per the relation, the voltage reduction is the most prominent methodology to degrade power dissipation. However, the voltage reduction is results in threshold voltage reduction which bows to the exponential increase in leakage power by using single edge triggered flip-flops, the clock frequency could be degraded which in further cut in half while preserving the rate of data processing and operation. Using lower clock frequency might explore into large power savings in the clocked portions of a circuit, which includes the clock distribution network.

2. CIRCUIT DESIGN

Shift registers are a type of sequential logic circuit, mainly used for storing digital data's. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop, then all the flip-flops are driven by a common clock pulse and all are set or reset simultaneously. The Parallel In Parallel Out (PIPO) shift register has three connections, the parallel input connection which determines what enters the flip-flop, the parallel output and the sequence clock signal. Similar to the Serial-in to Serial-out shift register, this type of register acts as a temporary storage device or as a time delay devices, with the amount of time delay being varies by the frequency of the clock pulses. In this type of register there are no interconnections between the individual flip-flops since no serial shifting of the data is required. The data is presented in a parallel format to the parallel input pins PA to PD and then transferred together directly to their respective output pins QA to QD by the same clock pulse. One clock pulse loads and unloads the register.

The D flip-flop is a modification of the clocked Set-Reset (SR) flip-flop. The D input goes directly into the S input and the complement of the D input goes to the Reset (R) input. The input D is sampled during the occurrence of the clock pulse. If it is one (on), the flip-flop is switched to the set state (unless it was already set). If it is 0 (off), the flip-flop switches to the clear state. The propagation delay is less compare with other existing work Flip-Flops (Sagar and Moorthy, 2012; Shaik and Suvarchala, 2013). The symbol of D flip flop is shown in the **Fig. 1** and the truth table of D flip flop is shown in the **Table 1**. The logic diagram of D flip flops are shown in **Fig. 2** and circuit diagram is shown in **Fig. 3**. The Structure of 4-bit PIPO Shift Register is shown in **Fig. 4**.

3. PERFORMANCE ANALYSIS

To evaluate the performance of proposed PIPO Shift Register using MODFET technology. Simulations are carried out using PSPICE tool in nominal conditions with operating frequency at 1GHz. Transient analysis of the proposed PIPO Shift Register using MODFET technology is shown in **Fig. 5**.

4. COMPARISON OF MOSFET AND MODFET SHIFT REGISTER

The proposed Parallel in Parallel Out (PIPO) Shift Register using MODFET D-flip flop is designed and compared with conventional Shift Register.

Table 1. Truth table for D flip-flop

Clk	D	Q
0	0	0
0	1	1
1	0	0
1	1	1

Table 2. Comparison of MOSFET and proposed shift register using MODFET

Device	Delay ($*10^{-12}$ Sec)	Power ($*10^{-7}$W)	PDP ($*10^{-17}$ J)
Con. MOSFET	259.00	3.45	8.94
Proposed MODFET	55.44	2.10	1.16

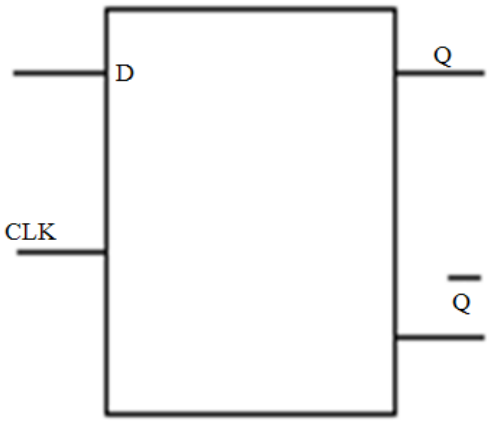


Fig 1. Symbol for an D flip flop

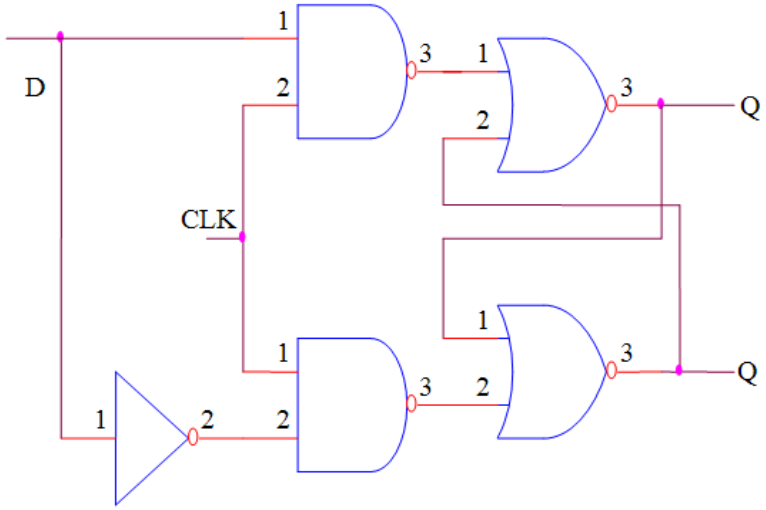


Fig. 2. Logic diagram Of D flip flops

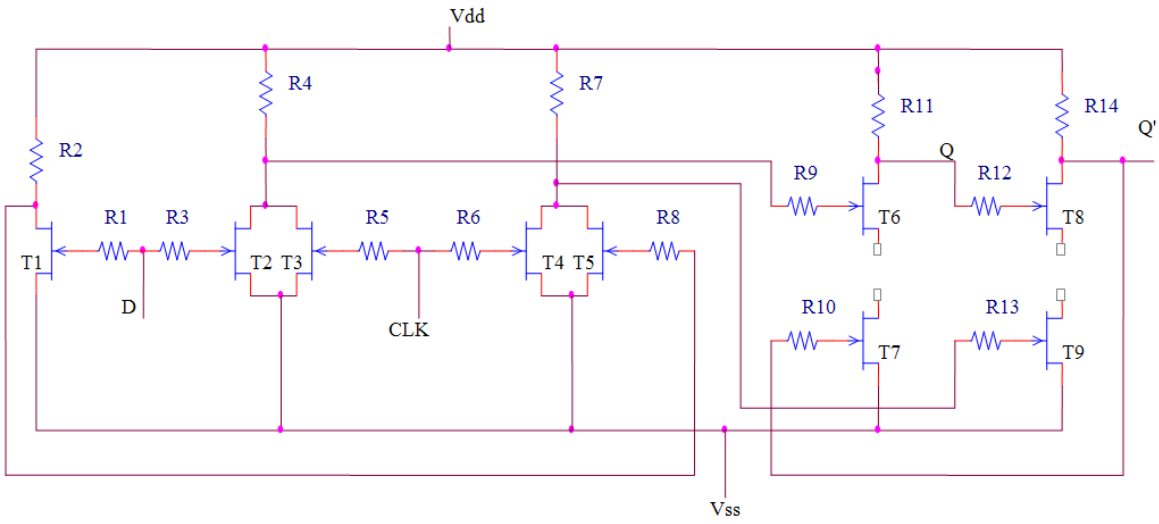


Fig. 3. Circuit diagram of d flip flop using modfet

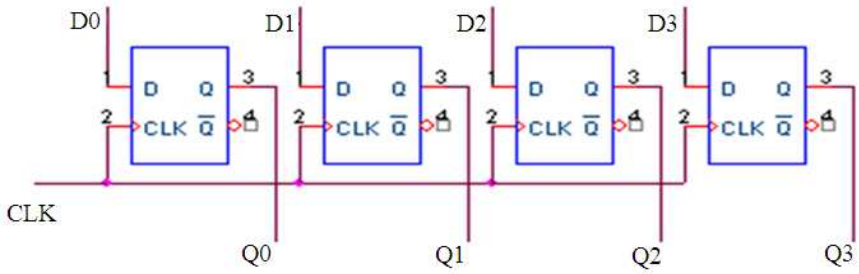
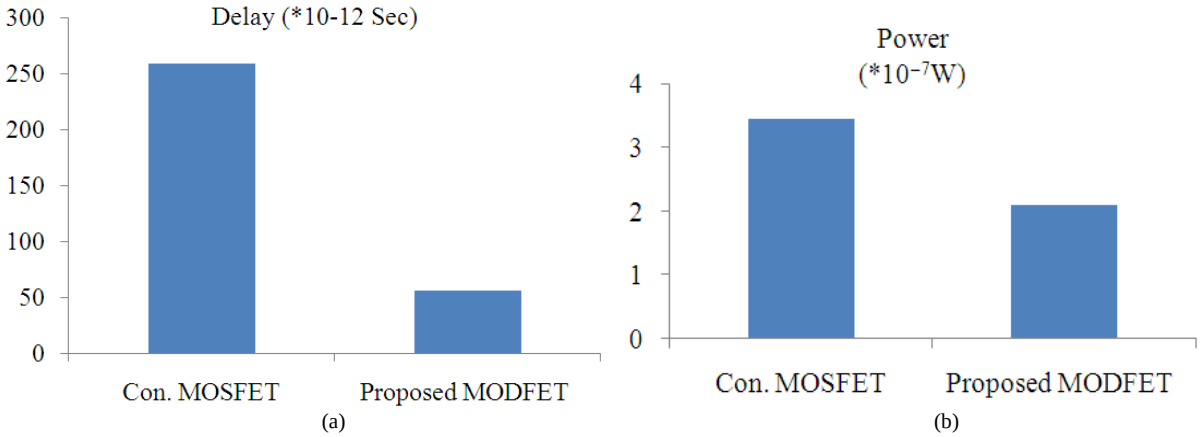
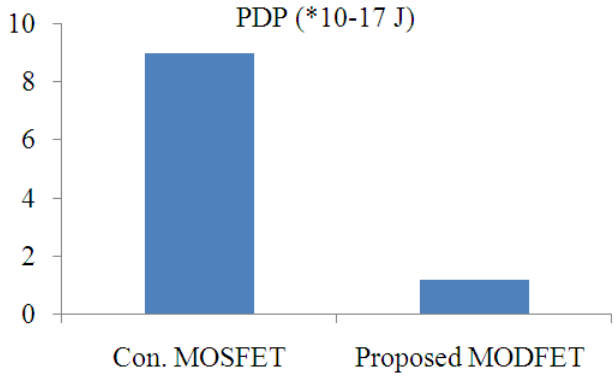


Fig. 4. Structure of PIPO shift register using MODFET

Fig. 5. Output waveform for proposed shift register



(a) (b)



(c)

Fig. 6. (a) Comparison of MOSFET and MODFET-Delay (b): Comparison of MOSFET and MODFET-Power (c) comparison of MOSFET and MODFET-PDP

Each Shift Register is optimized for power delay product. The proposed Shift Register is having lesser number of clocked transistors than the other Shift Register (Sridevi and Jayanthy, 2012; Saranya *et al*., 2013). Simulation results for delay, power, PDP and area at nominal conditions for proposed Shift Register then other existing Shift Register (Praveen *et al*., 2013; Sridevi and Jayanthy, 2012). Simulation results are summarized in **Table 2** and comparison graph is shown in the **Fig. 6a-c**.

5. CONCLUSION

This study aims to evaluate at a circuit and system level, the potential of MODFET in the MOS technologies for the realization of elementary logic functions. An optimal model for MODFET has been designed which is used to design flip flop and shift register circuits. The comparitive results of proposed MODFET and conventional MOSFET shows that MODFET circuits is about 5 times faster, the energy consumption is about 2 times lower and the Power Delay Product (PDP) is about 8 times lower then conventional MOSFET design.

6. ACKNOWLEDGEMENT

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