An Optimized Device Sizing of
Analog Circuits using Particle Swarm Optimization

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Abstract: Problem statement: Day by day more and more products rely on analog circuits to improve the speed and reduce the power consumption(Products rely on analog circuits to improve the speed and reduce the power consumption day by day more and more.). For the VLSI implementation analog circuit design plays an important role. This analog circuit synthesis might be the most challenging and time-consumed task, because it does not only consist of topology and layout synthesis but also of component sizing. **Approach:** A Particle Swarm Optimization (PSO) technique for the optimal design of analog circuits. Analog signal processing finds many applications and widely uses OpAmp based amplifiers, mixers, comparators. and filters. **Results:** A two-stage opamp (Miller Operational Trans-conductance Amplifier (OTA)) is considered for the synthesis that satisfies certain design specifications. Performance has been evaluated with the Simulation Program with Integrated Circuit Emphasis (SPICE) circuit simulator until optimal sizes of the transistors are found. **Conclusion:** The output of the simulation for the two-stage opamp shows that the PSO technique is an accurate and promising approach in determining the device sizes in an analog circuit.

Key words: Analog circuits, device sizing, opamp, SPICE

INTRODUCTION

Design of analog circuit has a vital role in the electronic system and the techniques for automating the analog circuit design started a decade ago. Because of the complexity in analog design, it has not been automated like digital design to a great extent. Circuit synthesis is the process of designing and constructing a network to provide a prescribed response to a specified excitation (Goh and Li, 2001). There are two phases in the design of analog circuit (Samrat *et al.*, 2009). First one is to construct the topology of the circuit and second one is to adjust the circuit parameters for a design specification, known as the circuit sizing. Cell sizing is the way in which designing an opamp by adjusting the transistor width, reference currents and compensation capacitor. This is a time-consumed process and in different technologies the scaling transistors bring out different results. Thus, analog circuit design automation techniques become essential to obtain solutions that satisfy the requested performance with the minimum time effort (Alpaydin *et al.*, 2003).

For a given schematic circuit and specifications, the sizes and biasing of all the devices have to be taken care in such a manner that the circuit meets the specifications with the optimal value. When an integrated circuit is fabricated the performance has some variations from that of the nominal design. This may occur due to several reasons and the two important error sources for this are the process variations and the mismatch (Hastings, 2006). The processes variations are caused by fluctuating process biases during the manufacturing and this will make the process parameters to change. Normally the process parameters are assumed to be the similar for all the devices on the same wafer, but may vary from wafer to wafer. Mismatch is caused by the local changes on the same chip, because the analog circuits rely on the close matching of a set of devices and the changes will degrade the performance of the circuit. When the process variations and the mismatch affect the analog circuit the performance of the circuit may fail to meet the desired specifications. So the circuit topologies and the set of design parameters are well identified that are less sensitive to such changes.

MATERIALS AND METHODS

Circuit design flow: Figure 1 shows the circuit design flow for an analog cell. For any design the specifications like power, gain, bandwidth, swing, of a circuit is given initially.

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Cell specifications

Topology selection

Circuit schematic

Device sizing

Sized circuit schematic

Layout

Cell layout
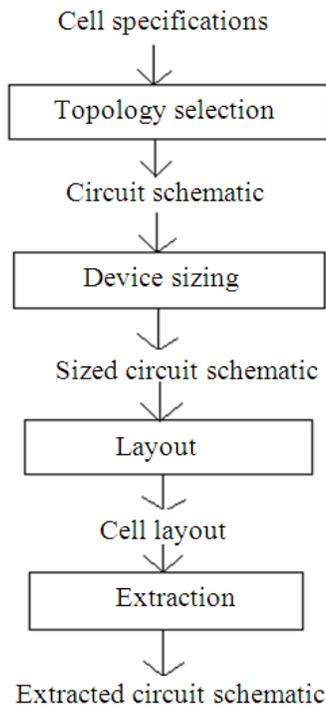
Extraction

Extracted circuit schematic

Fig. 1: Circuit design flow

In topology selection the circuit architecture is chosen and is a critical task. It requires good understanding of circuits and specifications. In the device sizing, choose the device sizes to meet the required specifications. Here the width and length of the transistors are desired. In the layout the sized schematic is converted into a physical representation which is ready for manufacturing. Then physical verification is done for the Design Rule Check (DRC) and the Layout Verses Schematic (LVS) check. Finally, in the extraction, the parasitic like resistances and capacitances are extracted by the layout. The circuits must be sized to fulfill with required various performance specifications to meet design objectives regarding area, power consumption, to assure a set of design constraints. For the past few years, advances in optimization techniques and design methodologies based on interactive computing have been made. The methods so far described suffer at least one of the following problems (Fakhfakh *et al*., 2009).

- Trapped easily at local minima
- Artificially convert the multi-objective problem to single-objective one
- Do fitness of an already determined feasible solution
- Not able to generate all the set of optimal solutions
- Depends on the form of the compromise surface

Related work: Review the prior work on improving the design strategy in analog circuits. Wang and Li (2006) proposed a two-layer evolutionary scheme based on Genetic Programming (GP) and Neural Network (NN), which uses a divide-and-conquer approach to design a low pass filter analog circuit. The new representation of the circuit is helpful to generate expectant circuit graphs. The algorithm can perform the circuits with dynamical size, circuit topology and component values in an efficient manner. Fakhfakh *et al*. (2010) proposed Particle Swarm Optimization (PSO) technique for the optimal design of analog circuits to solve both mono-objective and multi-objective discrete optimization problems. The technique is applied on a low noise amplifier with two operations. First maximizing the voltage gain and compute the Pareto front of a bi-objective problem and second minimizing the parasitic input resistance of a second generation current conveyor.

Oltean *et al*. (2009) proposed a method for analog circuit design optimization offered by computational intelligence techniques. The design objectives are expressed in a flexible manner using fuzzy sets. Neuro fuzzy systems are used to model the complex multi-variable and nonlinear circuit performance and the model satisfies high accuracy and low computation complexity.

Torres *et al*. (2009) presented a comparison of two different algorithms, a Univariate Marginal Distribution Algorithm for Analog Circuits (UMDA-AC) and a Genetic Algorithm for Analog Circuits (GA-AC). These algorithms are compared in performing the synthesis of topology and sizing of an analog low pass filter. Modeling of circuits is made by means of a linear representation technique with a variable length chromosome.

He *et al*. (2009) proposed a Multi-objective Simulated Annealing (MSA) approach to evolve logic circuits automatically with an extended matrix encoding method to improve automatic design and performance evaluation of logic circuits in efficiency and capability of optimization. This can be able to reflect eh potential performance of a circuit and reduce the risk of deleting a circuit with a good developing potential.

Tlelo-Cuautle *et al*. (2010) presented the art of applying evolutionary algorithms for the synthesis and sizing of analog Integrated Circuits. A survey of people working in this field and major advances and discoveries are summarized and finally several open research problems are listed to improve the electronic design automation tools for analog integrated circuits by applying evolutionary algorithms.

Kim *et al*. (2004) presented a technique for improving the accuracy of Geometric Programming

(GP) based analog circuit design optimization. Device modeling based on convex piecewise-linear function fitting is introduced to create accurate active and passive device models. Also, suggested a simple method to take the modeling error into account in GP optimization, which results in a robust design over the inherent errors in GP device models.

Fakhfakh *et al*. (2009) presented a novel heuristic for optimizing analog circuit performances and deals with generating the Pareto front using the topological properties of the feasible solution space. The heuristic allows generating optimal values of circuit parameters in reduced computation time and memory consumption and robustness of the algorithm was proved using specific difficult test problems.

Soto *et al*. (2010) presented a group of evolutionary mechanism for the design of analog circuits, embedded on a genetic algorithm that performs the synthesis of an analog filter. The algorithm interacts with SPICE, to evaluate the fitness of evolved circuits. To model an analog circuit, a linear representation is introduced and its corresponding reproduction operators that preserve the valid topological analog circuit class closed.

Das and Vemuri (2007) presented a genetic algorithm based automated circuit synthesis tool for passive analog circuits. It describes the procedure for developing both the circuit topology and the component values for a passive analog circuit comprising of R, L and C components from a given set of specifications. The novelty of the work pertains to the component value assignment procedure for the initial set of circuits and the crossover techniques employed.

Habal and Graeb (2011) presented a genetic algorithm based automated circuit synthesis framework for passive analog circuits. A procedure is developed for the simultaneous generation of both the topology and the component values for analog circuits comprising of R, L and C elements, from a given set of specifications. In this, the selection procedure chooses prospective parent circuits for mating on the basis of comparable fitness values and the crossover process comprises of exchanging well-defined sub-circuits, encompassing the whole design space, between the two chosen parent circuits.

Zhou *et al*. (2011) presented a fast analog circuit analysis algorithm for circuits being repeatedly modified and verified in product development. The algorithm reuses the circuit simulations on successive change in circuit analysis to achieve simulation operation reduction. The proposed algorithm increases the speed of the circuit simulation five to ten times over the direct simulations, with accuracy.
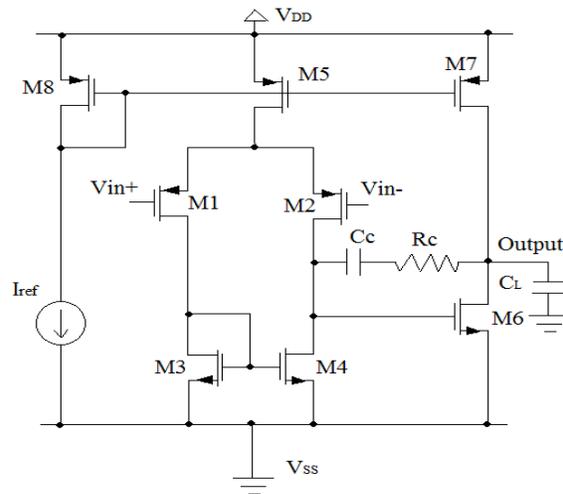

Fig. 2: Two-stage opamp

Liu *et al*. (2011) proposed a sampling-based yield optimization approach to determine the device size and is called Ordinal Optimization (OO)-based Random-scale Differential Evolution (ORDE) algorithm. The evolutionary algorithm uses differential evolution for global search and a random scale mutation operator for fine tuning to enhance the yield optimization.

Habal and Graeb (2011) presented a flow for the automatic synthesis of an analog circuit layout based on a schematic and a list of circuit design parameter values. The flow is driven by design, placement and routing constraints and every possible layout for each device in the circuit is analyzed. The layout with the optimal geometric features and smallest quantization error is considered. Finally, the flow is integrated with a deterministic nonlinear optimization algorithm to perform layout-driven circuit sizing.

Circuit design using PSO approach: Figure 2 shows a simple two-stage opamp circuit. Opamp is a power consuming building block in analog integrated circuit and the design of this analog circuit is a challenging and time consuming one. The two-stage opamp circuit provides better gain, output swing and is well suitable for low-voltage applications.

By the use of CAD tools the analog circuit design can be automated to enhance the design process to reduce the design time and design process complexity and also minimize the design and production cost. For the opamp the V_{DD} is assumed as 3.3 V and C_L is assumed as 1 pF. In this study, the opamp is optimized to get maximum gain, unity-gain bandwidth, slew-rate, phase margin and power consumption. The basic objective of the circuit design is to size the length and width of the CMOS transistors and also the values of the passive devices are adjusted simultaneously in the condition that the topology of the circuit is fixed.

Figure 3 shows the flow chart of PSO for the design of two-stage opamp circuit. PSO is a swarm intelligence technique and form a subset of metaheuristics. W and L are the width and length of the transistors. The optimal sizing of the opamp circuit consists of the following performance parameter functions:

W1 L1 W3 L3 W5 L5 W6 L6 L7 W8 L8 Cc Rc

A multiple candidate solutions coexist and cooperate with each other simultaneously in the metaheuristic PSO approach. Each solution is called a particle that flew within the problem search space looking for the optimal position to be placed (Torres *et al*., 2009). During each iteration, the particle changes its position based on its own experience and the experience gained by its neighboring particles. The entire particle will remember about its best position and is informed to the global version of the algorithm.

The PSO algorithm starts with the initialization of a swarm of particles in the search space. Each particle in the search space is represented by its position in the search space and the velocity of the particle. During each step or iteration all the particles adjusts their positions and velocities, which indicates the directions needed for the movement of the particles to improve the current position. The position changes of the particles in the search space are based on the social-psychological aspects of the individuals to emulate the success of other individuals (Yoshida *et al*., 2000).

In each generation, the velocity of each particle is calculated and the position of the next fitness function evaluation is updated by the following Eq. 1 and 2.

$$V_{t+1} = w * V_t + C_1 * rand\ (\ pbest\text{-}X_t\ ) + C_2 * rand\ (gbest\text{-}X_t\ ) \tag{1}$$

And:

$$X_{t+1} = X_t + V_{t+1} \tag{2}$$

Where:

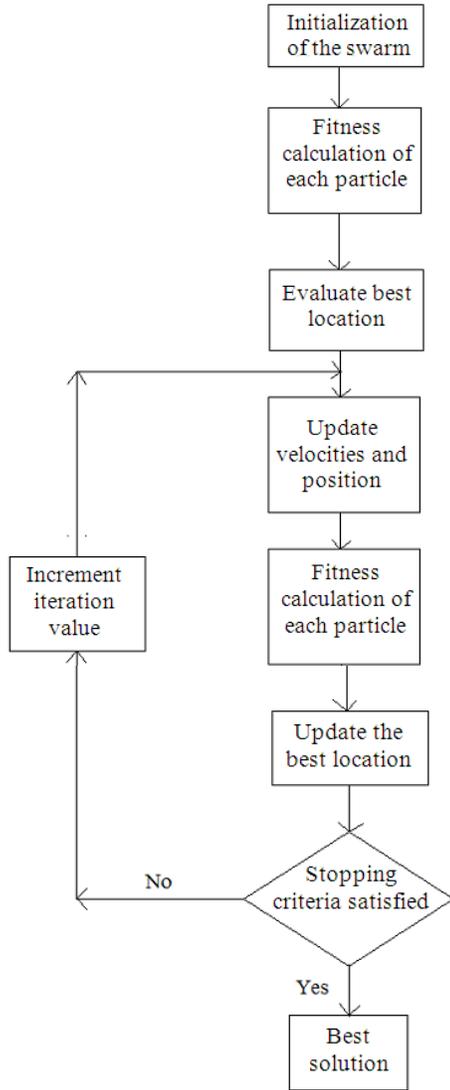|		
V_{t+1}	=	Updated velocity
w	=	Inertia weight
V_t	=	Old velocity
C_1 and C_2	=	Learning or acceleration factors = 2
Pbest	=	Best position of a given particle
Gbest	=	Best position by the particles neighbor
X_{t+1}	=	Updated position
X_t	=	Old position
rand	=	random numbers between 0 and 1

Fig. 3: Flowchart of PSO

Because of the enormous global search capability Evolutionary Algorithms (EAs) are used for the automatic design optimization by many researchers. PSO is a population-based searching technique inspired by natural mechanisms. This solves the optimization problems by emulating the flocking behavior of birds (Zhang *et al*., 2008). The representations of feasible solutions are employed by a swarm of particles in an efficient way and each particle has its own position and velocity. These two parameters are repeatedly updated by tracing the local best position and the global best position found so far. PSO has been used for many applications (Sushanta *et al*., 2008) and can considerably reduce the computational time.

PSO algorithm: A set of particles 'N' of swarm is defined initially and each particle is characterized by its position and velocity in the solution space. The position and velocity of ith particle (i = 1, 2, . . . , N) for an M dimension is represented as $X_i = \{x_{i1}, x_{i2}, x_{i3}, . . . , x_{iM}\}$ and $V_i = \{v_{i1}, v_{i2}, v_{i3}, ... , v_{iM}\}$ respectively. All the particles update its new position and velocity based on its own local best position (*pbes*t) and the best position of the entire (global) swarm (*gbest*). The following steps are evolved to get the optimum value.

Step 1: Initialize the position and velocity of each particle. For 'N' particles the position vector is given by $X(t) = \{X_1(t), X_2(t), X_3(t), . . . , X_N(t)\}$, where $Xi = \{x_{i1}, x_{i2}, x_{i3}, . . . , x_{iN}\}$ and the velocity vector is given by $V(t) = \{V_1(t), V_2(t), V_3(t), . . . , V_N(t)\}$, where $Vi = \{v_{i1}, v_{i2}, v_{i3}, . . . , v_{iN}\}$.

Step 2: Set the iteration process as 1.

Step 3: Based on the positions of each particle evaluate the objective function.

Step 4: Fitness value of each particle is compared with 'pbest' value. If the 'pbest' value is better than the previous value, then set the 'pbest' value to the current value.

Step 5: Compute the 'gbest' of the swarm from the best of all the particles 'pbest

Step 6: Update the velocity and position of each particle by the following equations:

$$V_{t+1} = w * V_t + C_1 * \text{rand} (pbest - X_t) + C_2 * \text{rand} (gbest - X_t) \text{ And:}$$
$$X_{t+1} = X_t + V_{t+1}$$

Step 7: Increment the iteration and proceed to step 3, until the stopping criteria is reached.

Step 8: Best solution is the 'gbest' value and evaluate the fitness value

RESULTS AND DISCUSSION

Simulations are carried out using the SPICE simulator for the two-stage opamp circuit in a Core 2 Duo, 2.2GHz, 2GB RAM system. The circuit has 8 CMOS transistors M1- M8, a compensation capacitor (Cc) and a load capacitor (C_L). The population size of the simulation is considered as 100, the maximum generation threshold is set to 80. Simulation shows that the PSO results in better characteristics than the desired objects. The circuit size vector and the performance characteristics are shown in the Table 1 and 2 respectively.

Table 1: Sizes of circuit components

W1	199u	L1	0.6u
W2	199u	L2	0.6u
W3	245u	L3	1.3u
W4	245u	L4	1.3u
W5	309u	L5	2u
W6	360u	L6	1.4u
W7	432u	L7	4.1u
W8	310u	L8	4.6u
Cc	3.2pf	Rc	545

Table 2: Obtained circuit values

Metrics	Obtained	Unit
Power	6.00	mW
Gain	81.23	dB
Phase Margin	60.08	Degrees
Slew Rate	288.00	V/us
Swing	2.44	V

CONCLUSION

This study applies a PSO-based device sizing approach to size the transistors in analog circuits, such as a two-stage opamp circuit. The two-stage opamp circuit has been validated using the SPICE simulator and the circuit configurations are predefined, so that the simulator can efficiently optimize the device sizes using the proposed optimization technique to meet the required objectives. This study can also be carried out by using the other optimization methods. PSO requires only less number of iterations to obtain the optimum solution. In this study, the parasitic wire capacitance during the implementation of layout generation is not considered and it can be carried out as future work. Moreover, analysis can also be carried out on other characteristics, such as noise and distortion behavior

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